



XA-9629  
PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Yutaka SHIMADA et al.

Appln. No.: 10/083,402

Group Art Unit: 1746

Filed: February 27, 2002

Examiner: Z. El Arini

For: MANUFACTURING METHOD OF SEMICONDUCTOR INTEGRATED  
CIRCUIT DEVICE

Allowed: January 22, 2004

Confirmation No.: 7383

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COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450  
Attn: Box Issue Fee

Sir:

The Examiner's Statement of Reasons for Allowance appears intended to address independent Claim 2. However, it is apparent that the other independent claims also distinguish patentably from the prior art based on the respective features recited therein.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been requested separately, such extension is hereby requested.

Respectfully submitted,

By: 

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MWS:lat

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